

# RedEagle

**Digital MCA** 

# Features

- Single and Dual 32k Digital MCA & Pulse Processor
- Provides Pulse Height Analysis (PHA with MSS and coinc/antocoinc), Time-stamped Lists and Multichannel Scaling (MCS) modes
- Ideally suited for high resolution spectroscopy applications utilizing HPGe, CZT, Silicon, and scintillation detectors such as NaI and LaBr<sub>3</sub>
- Supports Resistive Feedback and Transistor Reset preamplifiers as well as PMT anode signals
- On-board SSD memory supports List and Spectrum data storage capability (up to 200,000+ spectra)
- Web interface for quick retrieval of board details, firmware upgrading, and output data file browsing



### Overview

RedEagle is a stand-alone, single or dual digital 32k MCA, integrating input stage for the signal conditioning, fast analog-to-digital converter (ADC), digital processing algorithms, HV and Preamplifier Power Supply in a compact desktop form factor.

The instrument is suitable for high energy resolution semiconductor detectors, such as HPGe and Silicon detectors, for CZT, but also for scintillation detectors as Nal and LaBr<sub>3</sub>. It can manage positive and negative signals from resistive feedback or transistor reset preamplifier detectors; additionally accepts signals coming from PMT anodes.

### **Operating Modes**

RedEagle can be configured to operate in Pulse Height Analysis (PHA) acquisition mode, in Multichannel Scaling (MCS) acquisition mode, or in both PHA and MCS modes simultaneously. Multiple PHA spectra can be collected using Multispectral Scaling (MSS) mode with no data loss when switching to a new spectrum. The Time-Stamped List mode permits time and energy events to be saved either to on-board memory or to the host PC for offline analysis and post-processing. Analog input signals and internal digital filter outputs can be inspected via the Signal Inspector mode. Additionally, Compton/AntiCompton data acquisition is supported by taking advantage of the 2-input channel version.

#### I/O Equipment and Additional Features

RedEagle is equipped with I/O connectors which support several features beyond the standard MCA functionality. A DB25 I/O connector supports PHA Start/Stop, SCA, MCS, Coincidence/AntiCoincidence, Acquisition Start/Stop, ICR, Run Status, Sample Changer, and Sample Ready signals. The BNC connectors are reserved for Transistor Reset Preamp (TRP) inhibit, where the inhibit takes place on an external digital signal and can be extended in time via programming. Two SATA connectors allow for very precise multi-board synchronization, time stamp alignment, and system building via a simple daisy chain. Front Panel LED indicators inform the user as to board and I/O status, polarity of the power supply, and multi-board sync status. An OLED display provides general board information, real-time statistics on ICR, OCR, Real/Live/Dead Time, as well as details on the HVPS channel output.

#### HV and LV Power Supply

RedEagle can provide HV bias for up to two detectors. Three ranges of bias voltage and current, which are software configurable on a per-channel basis and hardware protected, allow the user to tailor the output V/I to specific detector types such as PMT (2 kV / 1 mA), HPGe (5 kV / 30  $\mu$ A), and Silicon (500 V / 50  $\mu$ A). The 2-input channel version of RedEagle allows the user to select the polarity configuration upon ordering: Positive-Positive, Negative-Negative, or Mixed. The 1-input channel version of RedEagle is provided with an HVPS configuration which includes 1-channel Positive Polarity and 1 -channel Negative Polarity. HV inhibit is supported with both positive and negative polarity. RedEagle also integrates low voltage outputs ( $\pm$ 12 V / 100 mA and  $\pm$ 24 V / 50 mA) to power preamplifiers. Detector Temperature and Nitrogen Levels may be monitored via external sensor interface.

#### Software

RedEagle is controlled by MC<sup>2</sup>Analyzer (MC<sup>2</sup>A), CAEN multi-board configuration and data acquisition software with basical spectrum analysis (ROI, energy calibration, FWHM, statistics), supporting all CAEN MCAs and digitizers running the DPP-PHA algorithm.

The embedded Linux-based ARM processor makes RedEagle well suited for unattended operations. Taking advantage of the available SDK tool, the user can customize the software (running embedded or on an external PC). The parameters of the processing algorithms can be tuned according to the detector or the application, and custom routines can be developed for automated operations, such as on-board spectrum and list recording, acquisition settings, logging and autonomous data acquisition when unconnected from external hosts.

### Connectivity

RedEagle can be controlled with a point-to-point direct connection through the USB 2.0 link and with a remote network connection by the Ethernet 10/100T port. The module also features a web interface that supports basic operations (sans spectroscopy software) by simply opening a web browser. The web interface is a quick and useful tool for finding basic board information (e.g. model type, serial number, firmware version, CPU load averages, real memory occupancy), for retrieving files saved on the onboard memory, for setting operational functions for each run (e.g. order, cut, copy/paste files, create and delete directories, user rights, etc.), and for managing network settings and upgrading firmware.

# **Technical Specifications**

Performance	SIGNAL PROCESSING         - Throughput tested up to 200 kcps         - Integral Non-Linearity (INL) 0.05% over the 99% of the full-scale range for Coarse Gain < 8; 0.1% for higher gains         - Differential Non-Linearity (DNL) < ±1% over the 99% of the full-scale range         - Dynamics down to 4 keV @ 3 MeV FSR (noise peak at the same height of Compton); measured with 7229P HPGe Canberra detector         - Pile-up Rejection and Live Time Correction; Pulse Pair Resolution: < 0.5 µs typical (depending on the fast discriminator shaping time)         - Dead-Time Correction error < 5% on the net area of a static reference source offended by a variable rate source ranging from 1 to 100 Kcps (at fixed Live Time Preset)         - Resolution best result is 0.61 keV @ 122 keV, 1.63 keV @ 1332 keV, measured with Cryo-Pulse 5 Plus Electrically Refrigerated Cryostat HPGe Canberra detector, equipped with iPa Preamp
On-board CPU and Logging	CPU - 1 ARM Cortex-A8 1 GHz (SDRAM Memory 512 MB DDR3L 800 MHz) running Linux Debian system - The embedded CPU is accessible for compiling customized routines and implementing unattended and automated operations by the provided SDK; 2 GB of space available for user installations SSD Memory - 32-GB microSD card, non-detachable; logging capability more than 200.000 spectra
Inputs	<ul> <li>INPUT (front panel) <ul> <li>Analog signal input connector; one unit in RedEagle single-input version; BNC type</li> <li>Accepts positive or negative signals from PMT anode or both Resistive Feedback and Transistor Reset detector preamplifier; 500 Ω input impedance.</li> <li>AC or DC coupling selectable by register with 5 µs, 11 µs or 33 µs possible value for the AC time constant; input range is 1 Vpp divided by the selected gain, 4 Vpp with x0.25 or 2 Vpp with x0.5 attenuation activated.</li> <li>HV INH (rear panel)</li> <li>High voltage inhibit connector; two units; BNC type.</li> <li>Inhibit function is duplicated on the rear PREAMP connector; DB9 type.</li> <li>Polarity of the HV INH signal is software selectable</li> <li>Positive polarity (default):</li> <li>the enable condition (cold detector) is an open circuit or active high, which means +2 V to + 24 V; inhibit condition (warm detector) is ground or active low, that is -24 V to -2 V</li> <li>Negative polarity:</li> <li>the enable condition (cold detector) is ground or active low, which means -24 V to -2 V; inhibit condition (warm detector) is an open circuit or active low, which means -24 V to -2 V; inhibit condition (warm detector) is an open circuit or active low, which means -24 V to -2 V; inhibit condition (warm detector) is ground or active low, that is +24 V to +24 V</li> <li>TRP INH / GATE (front panel)</li> <li>Transistor Reset Preamp/Gate Input connector; two units; BNC type; software selectable compatible logic TTL or NIM and function:</li> <li>- TRP-INH:Transistor Reset Preamplifier inhibit; the inhibit time value is determined by the longer of two conditions: either by the duration of the external signal or by the duration of an internal inhibit time.</li> <li>- GATE: Input signal acts as gate for coincidence/anticoincidence acquisition mode; event storage can be allowed/vetoed for the duration of the gate signal or for a programmable fixed time; programmable time ranges from 0.01 µs to 160 ms.</li> </ul> </li> <li>DC POWER IN (rea</li></ul>
	HV (rear panel) – Detector High Voltage power supply output connector; two units; SHV type. – Software selectable Voltage/Current output range options:

	<ul> <li>- 20 V to 2000 V @ 1 mA, suited for PMTs.</li> <li>- 20 V to 5000 V @ 30 μA, suited for HPGe detectors.</li> <li>- 20 V to 500 V @ 50 μA, suited for Silicon detectors.</li> </ul>
	– <b>Ripple</b> < 5 mVpp @ 2 kV < 10 mVpp @ 5 kV
	<ul> <li>Voltage / Current range may be configured in the software on a per-channel basis, so that the user can simultaneously bias identical or separate detector types (PMT, HPGE, Silicon) with a single RedEagle module.</li> <li>HVPS Polarity Output is selectable upon ordering (Positive-Positive, Positive Negative, Negative-Negative); the single-input version of RedEagle includes Mixed (Positive-Negative) HVPS output.</li> <li>Front Panel Polarity LED identifies positive or negative output for each channel by colour.</li> </ul>
Outpute	PREAMP (real panel)
Outputs	<ul> <li>Preamplifier power supply output connector; two units; DB9 type.</li> <li>Two power rails: ±12 V (± 2%) @ 100 mA ±24 V (± 2%) @ 50 mA.</li> <li>Ripple &lt; 5 mVpp</li> </ul>
	<ul> <li>Includes pins for 0 ÷ +10 Vdc level output, for detector temperature (PT100/PT1000 compliant) or Nitrogen level sensor readout, and for HVPS external inhibit input (in OR with HV INH connector; BNC type).</li> </ul>
	MON-OUT (front panel) – Analog output; BNC type – Provides a selection (software selectable) of internal analog probes: A copy of the input signal (4 Vpp FSR)
	<ul> <li>The Trapezoid</li> <li>The Trapezoid-Baseline</li> <li>The Fast Trigger</li> </ul>
	GPIO (rear panel)         - Connector for TTL I/Os; one unit; DB25 type (adapter to BNC available on request).         - Inputs (LVTTL, Zin 1 kΩ):
General Purpose I/Os	<ul> <li>Trigger Time Stamp Reset: External reset of the time stamp counter; minimum pulse width 15 ns; software programmable polarity.</li> <li>Acquisition Start/Stop: External Acquisition Start/Stop signal; minimum pulse width 15 ns; software programmable polarity; software programmable as edge sensitive (starts on first pulse and stops on second pulse) or level sensitive (starts on active signal and stops on inactive signal).</li> </ul>
	<ul> <li>External Trigger: External Trigger signal; minimum pulse width 15 ns; software programmable polarity; can be either a trigger for the channel or a trigger validation incase of acquisition in Coincidence mode.</li> <li>MCS Channel Advance: External Multichannel Scaler Channel Advance signal; minimum pulse width 15 ns; software programmable polarity; MCS channel advances upon external pulse.</li> </ul>
	<ul> <li>- MCS Sweep Advance: External Multichannel Scaler Sweep Advance signal; minimum pulse width 15 ns; software programmable polarity; the sweep currently in progress can be reset by external pulse.</li> <li>- Sample Ready: Sample Ready signal; minimum pulse width 15 ns; software programmable polarity; acquisition begins on an inactive signal, while an active signal delays the start of acquisition.</li> </ul>
	<ul> <li>– Outputs (LVTTL, do not require 50 Ω termination):</li> <li>– ICR: Incoming Count Rate; generates a positive pulse 150 ns wide at each event acquisition.</li> </ul>
	<ul> <li>SCA: Single Channel Analyzer; output pulse width 150 ns; software programmable polarity; a pulse is generated for each event whose energy stays between the Upper and Lower Level Discriminators (ULD, LLD).</li> <li>Sample Changer: Sample Changer signal; pulse width 140 ms; software programmable polarity; a pulse is generated for each sample advance command received by the instrument.</li> </ul>
	Front Panel LEDs – COMM: communication LED; colour green; turns on in case of activity over the USB or the ETHERNET channel. – STATUS: Status LED; bi-colour red/green:
	<ul> <li>- Continuous green: the board is ready to start.</li> <li>- Blinking green: the board is in RUN state.</li> <li>- Continuous red: the board is in BUSY state.</li> </ul>
LED Indicators	<ul> <li>HV: HVPS LED; red colour; turns on in event of an HV fail condition.</li> <li>INPUT: Trigger LED; colour green; turns on when a trigger is generated on the associated analog input channel.</li> <li>TRP-INH/GATE: Transistor Reset Preamplifier inhibit LED; colour green; turns on when the inhibit is active on the associated TRP input channel.</li> </ul>
	Rear Panel LEDs – INH: HVPS channel inhibit LED; colour red; turns on when inhibit is active. – OVC: HVPS channel over-current LED; colour red; turns on if the channel tries to draw more current than the programmed
	limit. – ON: HVPS channel enable LED; colour red; turns on when the HVPS channel is active. – POS: HVPS positive polarity LED; colour green; turns on in case of positive HVPS channel.
	<ul> <li>- NEG: HVPS negative polarity LED; colour yellow; turns on in case of negative HVPS channel.</li> <li>- SYNC: Synchronization LED; colour green; turns on when the clock of the board is locked with the clock signal on SYNC IN.</li> </ul>
	All settings are saved while the module is in power-off state; last configuration is automatically reloaded at power-on. – Signal Inspection: The analog input and the outputs of the digital filters can be inspected and plotted to optimize the algorithm parameters to attain the best possible spectrum.
Acquisition Modes	– PHA: By way of setting the programmable digital pulse processing parameters, the board will develop energy histograms that may be plotted and saved to file; spectrum can be binned at a configurable number of channels by the Conversion Gain control.
	<ul> <li>– MSS: Multispectral Scaling collects multiple PHA spectra; supports software or external TTL input Spectrum Advance command; not affected by dead-time while switching to a new spectrum.</li> <li>– Coincidence/Anticoincidence: configurable either for coincidence and anticoincidence between the board analog inputs (IN 0 and IN 1), or for external coincidence (GATE) and external anticoincidence (INH).</li> </ul>
	- Time-Stamped List: Raw energy and time tag data are provided and can be saved to file; 62-bit time tag counter; resolution of 10 ns; roll-over tracking event.
	- MCS:Multichannel Scaler mode; counts on fast discriminator, SCA or external inputs; the Start/Stop, the Channel Advance

	and the Sweep Advance can be on software command or on external signal (GPIO connector). – Unattended: Local storage of lists and spectra on the internal microSD memory without need of external PC control.
	GAIN <ul> <li>Through a combination of coarse and fine gain, the overall gain can be continuously adjusted from x0.8 up to x563.2 with respect to the 1 Vpp input range:</li> </ul>
	<ul> <li>- Coarse Gain: x1, x2, x4, x8, x16, x32, x64, x128, x256</li> <li>- Fine Gain: from x0.8 up to x2.2 in steps of 0.001</li> </ul>
	- By selecting the gain attenuation, the input range can be extended to 2 Vpp or 4 Vpp preventing saturation conditions, particularly for preamp signals with large DC offsets or transistor reset preamplifiers with a large output ramp dynamic
	range: - Gain Attenuation: x0.25, x0.5
	<ul> <li>Configuring the conversion gain defines the number of channels for the acquired spectrum:</li> </ul>
	- Conversion Gain: 256, 512, 1024, 2048, 4096, 8192, 16384, 32768 channels
	DC Offset
	The DC offset of the analog input is adjustable in the whole input range
	Algorithm
	– Input Signal
	Pulse Polarity: NEGATIVE or POSITIVE input polarity selection
	<ul> <li>Trapezoid Filter: serves for energy calculation; Trapezoid, Trapezoid-Baseline and Peaking signals can be displayed in Signal Inspection mode</li> </ul>
	<ul> <li>- Rise Time: trapezoid rise time corresponds to the shaping time of the traditional analog chain; configurable values between 0.02 µs and 37 µs</li> </ul>
Controls	- <b>Flat Top:</b> the flat region of the trapezoid, in which the energy is calculated; configurable values between 0.02 $\mu$ s and $\mu$ s
	<ul> <li>– Peak Delay: adjusts the point of the flat top where the energy value is calculated; the peaking (peak position) signal can be displayed in Signal Inspection mode; configurable values between 0% and 100%</li> <li>–PUR Protection Time: starts at the end of the flat top; plays a role in the pile-up rejection; configurable values between 0 µs and 81.84 µs</li> </ul>
	<ul> <li>– Pole/Zero Compensation: exponential decay time fine adjustment to avoid trapezoid overshoot or undershoot for a correct evaluation of the energy value:</li> </ul>
	– Decay Time: manually and automatically configurable between 0.1 $\mu s$ and 650 $\mu s$
	<ul> <li>Baseline Restorer: operates on the trapezoidal filter output to calculate the baseline by averaging a programmable number of points before the start of the trapezoid.</li> </ul>
	- Fast, Medium, Slow: manual setting of the baseline restorer to a fixed rate
	<ul> <li>Fast Discriminator: applies to time tagging and ICR; based on double triangular filter; manual and automatic setting of the threshold; time stamp resolution of 10 ns, 62-bit counter; trigger signal can be displayed in Signal Inspection mode.</li> </ul>
	– Fast TRG Shaping: configurable values between 0.01 $\mu s$ and 0.8 $\mu s$
	- Coupling & TRP: DC/AC coupling selection and Transistor Reset settings
	<ul> <li>- Coupling: DC coupling option for Charge Sensitive Preamplifiers; AC coupling option for Resistive Feedback and Transistor Reset Preamplifier with three selectable shaping constants: 5 μs, 11 μs and 33 μs (the trapezoid Decay Time must then be set accordingly.</li> <li>- Reset Length: inhibit time due to the reset discharge (AC coupling); applies to the Transistor Reset Preamplifier.</li> <li>- Pole Zero (%): analog pole zero compensation in case of Resistive Feedback Preamplifier (AC coupling)</li> </ul>
	<ul> <li>– MCS:</li> <li>– Dwell Time: 1 μs up to 4000 μs with resolution of 1μs</li> </ul>
ADC	RESOLUTION     SAMPLING RATE       14 bits     100 MS/s
Synchronization	SYNC IN (rear panel)         - Input connector for the synchronization of multiple RedEagle boards; one unit; SATA type         - Clock sync, time tag reset and list marker functions; daisy chainable to multiple boards in combination with SYNC OUT
	<ul> <li>SYNC OUT (rear panel)</li> <li>– Output connector for the synchronization of multiple RedEagle boards; one unit; SATA type</li> <li>– Daisy chainable to multiple boards in combination with SYNC IN</li> </ul>
	POWER (front panel) – Power on/off button; blue illuminated when the power is on
Active Buttons	RESET (rear panel) – Holding this button down for 3 seconds causes a global reset of the board (i.e. HVPS channels ramp-down and board resets)
Communication Interfaces	USB (rear panel) USB connector; USB 2.0 compliant; type mini-A. When connecting RedEagle to a host PC for the first time, the driver is automatically installed and is immediately recognize by the operating system(Windows® and Linux™), identifying the unit as an external storage device containing documentatio and software. USB cable included in the kit.
	<ul> <li>10/100 T (rear panel)</li> <li>Ethernet female connector; RJ-45 type.</li> <li>Supports 10 or 100 Mbit/s connection to a PC or ETH hub.</li> <li>FTP cable included in the kit.</li> </ul>

Monitoring Display	GRAPHIC DISPLAY (front panel) - Monochrome 1.3" OLED display only for monitoring usage Screen 1: Time acquisition data - Real Time [hh mm ss] / Live Time [hh mm ss] / Dead Time [%] - Screen 2: Readout data ICR [Hz], [kHz], [MHz] / OCR [Hz], [kHz], [MHz] / Dead Time [%] - Screen 3: HVPS data Vmon / Vset [V] / Imon[µA] - Screen 4: Network addresses - ETH / USB e1.e2.e3.e4 u1.u2.u3.u4; (ETH IP); (USB IP) Screen 5: Board Information - Model: DT500xx; Serial Number; Firmware version. BROWSE BUTTONS (front panel) - Channel select (0<->1): switches between the two analog input channels (if Screen 1 and Screen 2) or the two HPVS channels (if Screen 3) Screen Screen 3) Screen Select Button: scrolls through the screen options
Mechanical	EnclosureWeightAluminium with durable rubber front and rear supports1400 g.Size262 W x 66.2 H x 195 L mm³ (including connectors) 262 W x66.2 H x 171.6 L mm³ (without connectors)
Firmware	UPDATES – Firmware updates are available for free download on CAEN website: www.caen-india.in UPGRADE – Firmware can be upgraded via USB/ETHERNET through the Web Interface.

# Accessories

A387	Input Filter cable BNC female to BNC male – 25 cm
A998	SATA cable for RedEagle synchronization

# **Ordering Options**

Code	Description	
WDT4000XMAAA	DT4000M - REDEAGLE Dual Dig. MCA - 1 HVPS +5kV/30uA, 1 HVPS -5kV/30uA, 2 LVPS ±12V/100mA, ±24V/50mA	RoHS
WDT4000XNAAA	DT4000N - REDEAGLE Dual Dig. MCA - 2 HVPS -5kV/30uA, 2LVPS +/-12V/100mA, +/-24V/50mA	RoHS
WDT4000XPAAA	DT4000P - REDEAGLE Dual Dig. MCA - 2 HVPS +5kV/30uA, 2LVPS +/-12V/100mA, +/-24V/50mA	RoHS



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